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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/694,592
Filing Date: October 27, 2003
Appellant(s): PIHET, ERIC

Mark P. Weichselbaum, Reg. No. 43248
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 09/21/2010 appealing from the Office action mailed on 06/07/2010.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 12-28 and 30 are rejected and are under appeal. Claims 1-11 and 29 were cancelled.

(4) Status of Amendments After Final

Appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of appealed claims contained in the Appendix to the appellant's brief is correct.

(8) Evidence Relied Upon

6,034,995	EISELE	3-2000
5,124,990	WILLIAMSON	6-1992
6,535,028	BAKER	3-2003
4,516,248	BARCLAY	5-1985

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 12-22, 25-28, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eisele et al. (U. S. Patent No. 6,034,995 referred herein after Eisele) in view of Williamson (U. S. Patent No. 5,124,990).

As per claim 12, Eisele discloses: a method for checking for line faults in a bus system having at least two bus subscribers connected to a data bus for data communication between the subscribers, the data bus having at least two

bus lines, which comprises: (Eisele, fig. 1, col. 5, lines 57-64, “FIG. 1 shows diagrammatically three stations 1, 2 and 3 which are interconnected via three lines 11, 12 and 13.") where stations can be the "bus Subscribers" and lines 11,12, 13 can be “bus lines” as claimed;

configuring the bus subscribers with switches for placing the subscribers in a recessive state and a dominant state; (Eisele, col. 6, lines 17-21, “on the lines 11 and 12 in the case of open switches 6 and 7, therefore, will be referred to as the recessive state hereinafter and the state in the case of closed switches 6 and 7 as the dominant state.”, where switches are used to place bus subscribers in recessive or dominant state as claimed);

making available an internal high potential and an internal low potential in the bus subscribers; (Eisele, col. 6, lines 15-16, “the line 11 carries a high potential and the line 12 carries a low potential.”);

carrying out a check for line faults by comparing of voltage levels on the bus lines with threshold values related to one of an internal high level and an internal low level of the bus subscriber. (Eisele, fig. 2, col. 6, lines 28-51, "The line 11 is also connected to a comparator 22 which compares the potential on this line with a threshold value which is valued, taking into account tolerances, between the dominant and the recessive potential on the line 11. The comparator 22 generates a high signal on the line 32 if the potential on the line 11 exceeds the threshold value.").

Eisele does not specifically discloses ***a check for a line fault only when the at least one of the said bus subscribers is placed in said dominant state by said switching state of said switches;***

However, Williamson discloses the above claim limitations, (Fig. 6, element 614, 615, Col. 5, lines 1-9, where first and second pinned fault detection means checks for fault (short circuit) in the dominant state);

Therefore it would have been obvious to the one of ordinary skill in the art at the time of invention to incorporate Williamson's diagnostic method to Eisele's teaching because one of the ordinary skill in the art would have been motivated to provide fault tolerant serial communications in a network (Williamson, Col. 2, lines 26-27).

As per claim 13, claim 12 is incorporated and Eisele further comprises: providing a supply voltage referenced to an internal reference ground potential in the bus subscribers, the threshold values being greater than the

supply voltage; and (Eisele, fig. 1, col. 5, lines 66-67, col. 6, lines 1-3, "The line 11 is connected to ground via a resistor 14 and a switch. The line 12 is connected, via a resistor 15 and a further switch, to the operating voltage Vc which is derived from the supply voltage on the line 13 in the station.", col. 14, lines 1-13, "the line 11 carries the potential of the supply voltage;….. the line 11 carries a potential below said threshold voltage") where station can be "the bus subscriber" as claimed.

identifying a fault when one of the voltage levels on the bus lines is greater than the respective threshold value. (Eisele, col. 2, line 28-29, col. 1, lines 65-67, col. 2, lines 1-9, "comparator which is coupled to both lines in order to subtract the potential on the first line from the potential on the second line and to output an output signal of a first value via a first comparator output if the difference formed by the subtraction exceeds a first threshold value,") where voltage difference of two potentials can be "one of the voltage level on the bus line" as claimed and when the difference exceeds the threshold voltage, fault is identified as claimed.

As per claim 14, claim 13 is incorporated and Eisele further comprises identifying a fault when one of the voltage levels on the bus lines is greater than the respective threshold value during a predetermined number of successive dominant states of the bus subscriber carrying out the fault identification. . (Eisele, col. 1, lines 65-67, col. 2, lines 1-9, col. 14, lines 14-36, "the line 12 carries the potential of the supply voltage which is detected by the comparator 25, also having a threshold voltage of 7.3 V with respect to

ground……..one of the two lines carries a dominant signal … for a predetermined period of time").

As per claim 15, claim 12 is incorporated and Eisele further comprises: comparing the voltage levels on the data lines with one another for detection of transmitted data; and upon detection of a fault on one of the data lines, carrying out detection of transmitted data by comparing the voltage level on the other one of the data lines with a threshold value related to one of the internal high potential and the internal low potential. (Eisele, col. 2, lines 10-27, "a comparator which forms not only the difference between the potentials on the two lines but also compares this difference with a given first threshold value, the transmitted data signal..... each line is connected to a low potential or a high potential via a resistor") where one of the two lines interrupted means "fault detected" as claimed.

Claim 16 has similar limitations as claim 13 and claim 15 and therefore is rejected under the same reasons set forth in rejection of claim 13 and claim 15 above.

Claim 17 has similar limitations as claim 15 and claim 14 and therefore is rejected under the same reasons set forth in rejections of claim 14 and claim 15 above.

As per claim 18, a bus system, comprising:

a data bus having at least two bus lines; and (Eisele, fig 1, bus lines 11, 12 and 13, col. 5, lines 58-60, “three lines 11, 12 and 13”);

at least two bus subscribers coupled to said data bus for serial data transfer of binary data between said bus subscribers, at least one of said bus subscribers having: (Eisele, fig 1, stations 1, 2 and 3, col. 3, lines 2-5, col. 5, lines 58-64, “three stations 1, 2 and 3 which are interconnected via three lines 11, 12 and 13….the data is transmitted”) where station can be "bus subscriber" as claimed;

at least one control unit; (Eisele, fig 1, element 5, col. 6, lines 5-15, “the station 2 comprises a control device 5”) where control device can be “control unit” as claimed;

Switches for assuming a switching state placing the one of said bus subscribers in a dominant state; (Eisele, col. 6, lines 17-21, “the state in the case of closed switches 6 and 7 as the dominant state.”, where switches are used to place bus subscribers in recessive or dominant state as claimed);

at least one transceiver for at least one of transmission and reception of data signals; and (Eisele, col. 4, lines 52-55, “At least in stations which not only are capable of receiving but also of transmitting data each line is coupled, via an associated switch,”) where associated switch can a “transceiver for transmission and reception of data signals" as claimed;

at least one fault identification device configured to: (Eisele, fig. 2 ,element 26 and 27, col. 6, lines 39-42, “The line 31 is also connected to two fault detection

circuits 26 and 27 “) where fault detection circuit can be “fault identification device” as claimed.

cause the one of said bus subscribers to be able to assume a recessive state and the dominant state (Eisele, col. 6, lines 17-21***),***

make available an internal high potential and an internal low potential in the one of said bus subscribers (Eisele, col. 6, lines 15-16, “the line 11 carries a high potential and the line 12 carries a low potential.”);

carry out a check for line faults by comparing voltage levels on the bus lines with threshold values related to one of an internal high level and an internal low level of the one of said bus subscribers (Eisele, fig. 2, col. 6, lines 28-51)***;***

Eisele does not specifically discloses ***a check for a line fault only when the at least one of the said bus subscribers is placed in said dominant state by said switching state of said switches;***

However, Williamson discloses the above claim limitations, (Fig. 6, element 614, 615, Col. 5, lines 1-9, where first and second pinned fault detection means checks for fault (short circuit) in the dominant state);

Therefore it would have been obvious to the one of ordinary skill in the art at the time of invention to incorporate Williamson’s diagnostic method to Eisele’s teaching because one of the ordinary skill in the art would have been motivated to provide fault tolerant serial communications in a network (Williamson, Col. 2, lines 26-27).

As per claim 19, claim 18 is incorporated and Eisele further comprising at least one fault detection device comparing at least one voltage level on one of said bus lines with a threshold value related to one of the internal low level and the internal high level and providing a fault signal. (Eisele, fig. 3, col. 2, lines 10-27, "a comparator which forms not only the difference between the potentials on the two lines but also compares this difference with a given first threshold value, the transmitted data signal..... each line is connected to a low potential or a high potential via a resistor", col. 8, lines 23-26, "A fault signal is thus generated on the corresponding line 36a or 36b").

Claim 25 has similar limitations as claim 19 and therefore is rejected under the same reasons set forth in rejections of claim 19 and further ***means for detecting*** can be fault detection circuit (Eisele, fig. 2, element 27 and 26) ***means for comparing*** can be a comparator (Eisele, fig. 2, element 21).

As per claim 20, claim 19 is incorporated and Eisele further discloses: wherein said at least one fault detection device is:
a first fault detection device comparing a voltage level on one of said data lines with a first threshold value and provision a first fault signal; and (Eisele, col. 6, lines 29-59, "it subtracts the potential on the line 12 from that on the line 11 and compares the difference of correct sign with a first threshold value….generates a signal on the line 34..") where voltage difference in line potentials can be "a

voltage level on one of said data lines" as claimed. Line 34 is connected to the lower fault detection circuit 27;

a second fault detection device comparing a voltage level on the other one of said data lines with a second threshold value and providing a second fault signal. (Eisele, col. 2, lines 36-46, "a second comparator which is coupled to the first line in order to generate an output signal of the first value on a second comparator output if the potential on the first line exceeds a second threshold value", col. 7, lines 12-15, "The upper fault detection circuit 26 generates a fault signal on an output line 36a").

Claim 26 has similar limitations as claim 20 and therefore is rejected under the same reasons set forth in rejections of claim 20 and further ***means for detection*** can be fault detection circuit (Eisele, fig. 2, element 27 and 26) ***means for comparing*** can be a comparator (Eisele, fig. 2, element 21).

As per claim 21, claim 20 is incorporated and Eisele further comprising a first data detection device for detection of transmitted data, said first data detection device comparing voltage levels on said bus lines and providing a first data signal. (Eisele, col. 2, lines 10-27, "a comparator which forms not only the difference between the potentials on the two lines but also compares this difference with a given first threshold value, the transmitted data signal..... each line is connected to a low potential or a high potential via a resistor") where voltage

difference in line potentials can be "a voltage level on one of said data lines" as claimed and one of the two lines interrupted means "fault detected" as claimed.

Claim 27 has similar limitations as claim 21 and therefore is rejected under the same reasons set forth in rejections of claim 21 and further ***means for detection*** can be fault detection circuit (Eisele, fig. 2, element 27 and 26) ***means for comparing*** can be a comparator (Eisele, fig. 2, element 21).

As per claim 22, claim 21 is incorporated and Eisele further comprising:
at least one second data detection device for detection of transmitted data, said second data detection device comparing a voltage level on at least one of said data lines with at least one threshold value related to the internal low level to provide at least one second data signal; and (Eisele, col. 2, lines 36-46, "a second comparator which is coupled to the first line in order to generate an output signal of the first value on a second comparator output if the potential on the first line exceeds a second threshold value", col. 7, lines 12-15, "The upper fault detection circuit 26 generates a fault signal on an output line 36a");
a switch switching between said first data signal and said at least one second data signal as a function of said at least one fault signal. (Eisele, col. 2, lines 35-46, "a second comparator which is coupled to the first line in order to generate an output signal of the first value on a second comparator output if the potential on the first line exceeds a second threshold value .....memory being coupled to a switch for

switching the data output from the first comparator output to the second comparator output") where second comparator generates a fault signal as claimed.

Claim 28 has similar limitations as claim 22 and therefore is rejected under the same reasons set forth in rejections of claim 22 and further ***means for detection*** can be fault detection circuit (Eisele, fig. 2, element 27 and 26) ***means for comparing*** can be a comparator (Eisele, fig. 2, element 21). And a ***means for switching*** can be a switch (Eisele, fig. 1, element 5).

As per claim 30, a bus system, comprising:

a data bus having at least two bus lines; and (Eisele, fig 1, bus lines 11, 12 and 13, col. 3, lines 2-5, col. 5, lines 58-60, "three lines 11, 12 and 13");

at least two bus subscribers coupled to said data bus for serial data transfer of binary data between said bus subscribers, at least one of said bus subscribers configured (Eisele, fig 1, stations 1, 2 and 3, col. 5, lines 58-64, "three stations 1, 2 and 3 which are interconnected via three lines 11, 12 and 13….the data is transmitted") where station can be "bus subscriber" as claimed;

to assume a recessive state and a dominant state and having (Eisele, col. 6, lines 16-21, "in the case of open switches 6 and 7, therefore, will be referred to as the recessive state hereinafter and the state in the case of closed switches 6 and 7 as the dominant state.");

internal high and low potentials; (Eisele, col. 6, lines 15-16, "the line 11 carries a

high potential and the line 12 carries a low potential.");

internal high and low levels; (Eisele, col. 6, lines 22-27);

at least one control unit; (Eisele, fig 1, element 5, col. 6, lines 5-15, "the station 2 comprises a control device 5") where control device can be "control unit" as claimed;

Switches for assuming a switching state placing the one of said bus subscribers in a dominant state; (Eisele, col. 6, lines 17-21, "the state in the case of closed switches 6 and 7 as the dominant state.", where switches are used to place bus subscribers in recessive or dominant state as claimed);

at least one transceiver for at least one of transmission and reception of data signals, said transceiver connected to said control unit; and Eisele, col. 4, lines 52-55, "At least in stations which not only are capable of receiving but also of transmitting data each line is coupled, via an associated switch,") where associated switch can a "transceiver for transmission and reception of data signals" as claimed;

at least one fault identification device connected to at least said transceiver and carrying out: (Eisele, fig. 2 ,element 26 and 27, col. 6, lines 39-42, "The line 31 is also connected to two fault detection circuits 26 and 27 ") where fault detection circuit can be "fault identification device" as claimed;

a check for line faults by comparing voltage levels on said bus lines with threshold values related to one of said internal high level and said internal low level. (Eisele, fig. 2, col. 6, lines 28-51, "The line 11 is also connected to a

comparator 22 which compares the potential on this line with a threshold value which is valued, taking into account tolerances, between the dominant and the recessive potential on the line 11. The comparator 22 generates a high signal on the line 32 if the potential on the line 11 exceeds the threshold value.");

Eisele does not specifically discloses ***a check for a line fault only when the at least one of the said bus subscribers is placed in said dominant state by said switching state of said switches;***

However, Williamson discloses the above claim limitations, (Fig. 6, element 614, 615, Col. 5, lines 1-9, where first and second pinned fault detection means checks for fault (short circuit) in the dominant state);

Therefore it would have been obvious to the one of ordinary skill in the art at the time of invention to incorporate Williamson's diagnostic method to Eisele's teaching because one of the ordinary skill in the art would have been motivated to provide fault tolerant serial communications in a network (Williamson, Col. 2, lines 26-27).

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eisele and Williamson in view of Barclay et al (U. S. Patent No. 4,516,248 referred herein after Barclay)

As per claim 23, claim 18 is incorporated and Eisele further discloses: wherein

said data bus serially transmits binary data and is in the form of a differential,

(Eisele, col. 5, lines 58-64)

Eisele does not specifically disclose:

Said data bus transmits duplex signals with two-wire data bus having two bus lines twisted with one another.

However, in the analogous art Barclay discloses:

Said data bus transmits serially by duplex signals with two-wire data bus having two bus lines twisted with one another. (Barclay, fig. 3, lines 58 and 60, col. 10, lines 54-55, "Twisted pair wire is the least expensive means of data transmission", col. 7, lines 62-65, "the user interface circuit 30 is full duplex"). Therefore it would have been obvious to the one of ordinary skill in the art at the time of invention to incorporate Barclay's data transmission method to Eisele's and Williamson's teaching because one of the ordinary skill in the art would have been motivated to a high performance data communication peer network. (Barclay, col. 1, lines 7-8).

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eisele and Williamson in view of Baker (U. S. Patent No. 6,535,028).

As per claim 24, claim 18 is incorporated and Eisele does not specifically disclose***: wherein the bus system is a CAN bus system.***

However, Baker discloses: ***the bus system is a CAN bus system***. (Baker, col. 1, lines 6-8, "circuit for a differential serial bus, such as a CAN ("Controller Area Network") bus system."

Therefore it would have been obvious to the one of ordinary skill in the art at the time of invention to incorporate Baker's bus system to Eisele's and Williamson's teaching because one of the ordinary skill in the art would have been motivated to operate in noisy electrical environments with a high level of data integrity, and its open architecture and user-definable transmission medium make it extremely flexible. (Baker, col. 1, lines 12-15).

(10) Response to Argument

1. In the appeal brief dated 09/21/2010 appellants presented two main arguments, which are addressed below in the order in which they were presented,

First argument and Examiner's Response

2. **On page 10 of the brief appellants argue that the one of ordinary skill in the art concerned with designing a parallel data bus, such as that taught by Eisele et al. would not refer to a teaching of a ring network, such as taught by Williamson.**

The examiner respectfully disagrees. It was already admitted in the previous office action that Eisele et al. has parallel network data transmission but is silent about the step of carrying out a check for a line fault by a bus subscriber

only when the bus subscriber is placed in the dominant state, **although the Williamson et al. has serial (ring) network transmission but it was brought in to teach a checking line fault when the bus subscriber is placed in the dominant state by the switches as claimed (Williamson, Fig. 6, element 614, 615, Col. 5, lines 1-9, where first and second pinned fault detection means checks for fault (short circuit) in the dominant state).** Appellants seem to focus on the fact the Williamson specifically does not have parallel transmission.

Appellants has not provided any proof or any elaboration as to why two different type of networks with different topology and different protocol will not work, Appellants have simply made conclusive and opinion statement without providing any facts to the examiners remarks. Examiner believes that one in the ordinary skill in art would make a parallel-to-serial conversion at a computer interface when sending data from a computer system into a network and a serial-to-parallel conversion at a computer interface when receiving information from a network for example A special computer chip known as a universal asynchronous receiver transmitter (UART) acts as the interface between the parallel transmission of the computer bus and the serial transmission of the serial port and JTAG to realize faster speeds and greater performance.

Second argument and Examiner's Response

3. ***The appellants argue that the data bus in Eisele et al. does not discrete portions located only between a particular receiver and a particular transmitter.***

It is already admitted in the previous office action that Eisele et al. has parallel network data transmission and Williamson et al. has serial data transmission. As provided the description of the UART in the response of the first argument, UART is a hardware that translates data between serial to parallel form. It is necessary that the appellants to provide the facts and solid reasoning or evidence to prove that the applying a feature of a ring network to a parallel data bus would not work.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Kamini Patel/
Examiner, Art Unit 2114

/Scott T Baderman/
Supervisory Patent Examiner, Art Unit 2114

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